(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 650 123 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
03.02.1999 Bulletin 1999/05

(51) Int Cl.[6]: **G06F 11/26**, G06F 11/24

(21) Application number: **94102885.4**

(22) Date of filing: **25.02.1994**

(54) Integrated logic circuit with scan path

Integrierte Logikschaltung mit Abtastpfad

Circuit logique intégré avec trajet d'analyse

(84) Designated Contracting States:
DE FR GB IT NL

(30) Priority: **25.02.1993 GB 9303758**

(43) Date of publication of application:
26.04.1995 Bulletin 1995/17

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EP-A- 0 408 299 **EP-A- 0 481 097**
EP-A- 0 498 534

- **PATENT ABSTRACTS OF JAPAN vol. 7, no. 274 (P-241) 7 December 1983 & JP-A-58 154 038 (NIPPON DENKI) 13 September 1983**
- **Week 8745, Derwent Publications Ltd., London, GB; AN 87-318899 ANONYMOUS 'Test register for scan-path or self-test environment' & RESEARCH DISCLOSURE, vol.282, no.8, 10 October 1987, EMSWORTH GB**

EP 0 650 123 B1

Printed by Jouve, 75001 PARIS (FR)

Description

[0001] The present invention relates to integrated logic circuits and in particular to a circuit and a method of exercising such circuits as defined in the precharacterizing portions of claims 1 and 2, respectively.

[0002] Very large scale integration techniques allow a large amount of logic to be realized by a single device. Such a device can be difficult to test, however, due to its complexity in relation to the limited access to circuit nodes provided by external device pins. Nonetheless it is normally possible to provide a functional test by driving device inputs with known test patterns and monitoring outputs for a consistent response. In the case of combinatorial logic, a series of test patterns may be defined which fully exercises all possible device states to provide an exhaustive test which can form the basis of a practical test if the number of inputs is not excessive. For devices having storage elements the task can be significantly more complex, but by clocking elements to known states as part of testing, worthwhile test patterns are still possible. Unfortunately, the derivation of a substantially exhaustive test pattern can become a design exercise rivaling that of the device itself in complexity and represents a significant cost to which the cost of equipment required in practice to generate the test vectors and that of testing time must be added. Such costs can be prohibitive for low production quantities and a limitation in, for example, the application specific device market.

[0003] In an attempt to overcome this problem 'Design for Test' philosophies have been developed and are aimed at making devices more testable without recourse to full test vector generation. For example, one such philosophy is based upon arranging that all storage elements within a device are configurable, in a special test mode of device operation into one or more chains and able to receive clock signals so that the chain behaves as a shift register. The device, whatever its intended function, may then be regarded as relatively simple (i.e. easily tested) combinatorial blocks between shift register stages providing inputs and outputs to the blocks. By providing an input pin at one end of the chain so that register stages may be loaded and an output pin at the other end so that stages may be interrogated, testing independent of knowledge of overall intended device functionality is possible. Of course, external equipment to generate the test vectors to be loaded and examine the resultant output is still required, but at least the test vector derivation task has been simplified. Reference may be made to IEEE Standard 1149.1-1990 which was developed under the auspices of the Joint Test Action Group (JTAG). The approach itself has become known as "JTAG".

[0004] The Design for Test philosophy may be useful even where devices cannot be internally configured to provide scan paths. According to one aspect of JTAG, for example, devices are prodded with scannable storage elements at least at key input and output pins. When several such devices are connected, the overall circuit may be tested in accordance with scan techniques. A similar technique (boundary scan) can be employed to verify device interconnection and an arrangement for testing a circuit assembled on a printed circuit board is described in UK Patent Application 92 17728 filed on 20 August 1992.

[0005] Apart from a one off functional test to a particular production device, there is the issue of reliability. To determine reliability, an accelerated life test might be performed on a batch of devices. Such a test might involve prolonged operation under high stress conditions (high temperature, maximum allowable input values, high frequency, etc) in an attempt to promote the onset of faults that would appear only much later in normal use. A similar approach can be taken in production to eliminate specimens that would fail prematurely in normal use.

[0006] A feature of accelerated life testing is that devices under test need to be exercised at the same time as they are exposed to the stressful environment. Typically, it is not cost effective or practicable to place functional testing equipment within the environmental chamber that establishes the test conditions so limited functionality test fixtures are used, arranged to exercise the devices as much as possible in the circumstances; a few test patterns stored in read only memory, together with some clock generation, for example. Unfortunately, the full test patterns discussed earlier although they fully exercise the device, will not typically be useful (too large, complex or non-existent) meaning that yet another design exercise has to be undertaken to produce the exercise pattern, adding further to design costs.

[0007] Patent Abstracts of Japan, Volume 7, No. 274 (P - 241); JP-A-58154038 describes a complex functional block composed of flip-flops which can be configured as a parallel register, a shift register, a linear feedback shift register, or a signal line can bypass the flip-flop in response to control signals, C1 and C2.

[0008] WEEK 8745, Derwant Publications Ltd., London, GB, AN 87-318899, "Test Register for Scan-Path or Self-Test Environment", & RESEARCH DISCLOSURE, vol. 282, no. 8, 10 October 1987, EMSWORTH, GB describes a complex functional block which can be configured as a parallel data register, a serial scan register, a linear feedback shift register or a parallel signature analyzer in response to three control signals, C0, C1 and C2.

[0009] The present invention has been made in an attempt to ameliorate the accelerated life design overhead.

[0010] According to the present invention in a first aspect thereof there is provided an integrated logic circuit as mentioned in the beginning and having the features of the characterizing portion of claim 1.

[0011] According to the present invention in a second aspect thereof there is provided a method as mentioned

in the beginning and having the features of the characterizing portion of claim 2.

[0012] In order that features and advantages of the present invention may be more fully appreciated, embodiments will now be described with reference to the accompanying diagrammatic drawing figures of which:

Figure 1 repesents a shift register latch;
Figure 2 represents a logic circuit for integration designed in accordance with "Design for Test" principles;
Figure 3 represents a scannable chain of shift register latches incorporating the present invention;
Figure 4 shows part of an alternative embodiment;
Figure 5 represents a block diagram of a "Design for Test" device;
Figure 6 and Figure 7 are details of some logic present in the device of Figure 5; and
Figure 8 shows an accelerated life test configuration.

[0013] In an integrated logic circuit to be designed in accordance with design for test principles, storage elements are provided by shift register latches. In a shift register latch (Figure 1) a signal present at an input 10 may be clocked ot a master latch formed of two inverters (15, 16) by application of a master clock pulse to a master clock transistor 11. The information is further clocked by applying a slave clock pulse to slave clock transistor 17 to latch a slave formed by two inverters (18, 19) which provides a latched output at 100. It will be appreciated that the arrangement described thus far provides a master slave latch of conventional behavior. An alternative input 12 may be latched by using scan clock transistor 14 in conjunction with slave clock transistor 17, hence either main input I_1 or scan input I_S will be latched depending upon whether the master or the scan clock is used.

[0014] The logical functionality of the desired circuit is designed by using main input I_1 in conjunction with output 100 in a plurality of shift register latches in combination with combinatorial logic gates. As part of Design for Test however, the shift register latches are additionally connected in series with each output 100 connecting to the auxiliary scan input I_S of a different shift register latch. Thus, by entering a mode wherein the scan clock is used instead of the master clock, data may be transferred from one shift register latch to the next along what is referred to in the art as a scan path. By providing an overall scan input and an overall scan output, the contents of the shift register latches may be loaded and interrogated.

[0015] The arrangement is shown more clearly in Figure 2, wherein a plurality of circuit inputs I (20) are shown connected in the first place to a bank of shift register latches 23 then onto a block of combinatorial logic 26 and then to a further bank of shift register latches 24. In this way, the functionality of the desired logic integrated circuit is provided. In the present case, a further block of combinatorial logic 27 and together with a yet further bank of shift register latches 25 provides the eventual outputs O (204). Master and slave clocks are, in use, provided to the circuit by inputs 29 and 200 respectively which are shown feeding a clock generator 28. Not shown are the internal clock conditioning and gating circuits which provide clock signals via internal interconnections to each and every set register latch as described with respect to Figure 1. In alternative arrangements, all clock signals may be internally derived from a single externally applied clock.

[0016] The shift register latches are shown symbolically connected together one to the next such that output 100 of shift register latch 21 is connected to scan input 12 of shift register latch 22 and this connection is repeated for all shift register latches in the bank. The banks themselves are interconnected as shown such that there is an overall single scan input 205 and overall single scan output 206 for the entire device.

[0017] When the device is to operate normally, clock signals are fed to the master and the slave to control the operation of the circuit in response to inputs applied to the input pins 20 to generate the required outputs at the output pins 204 in accordance with the design specification. By applying suitable control signals via an input 203 to scan test control logic 201, an alternative mode of operation may be entered wherein a scan clock replaces the master clock. For example, when it is desired to test the circuit one might proceed as follows.

1. Load the shift register latches with predetermined test data by applying a serial data stream to the scan input 205, the scan clock to input 202 and the slave clock to input 200. At the end of this, known inputs will be applied to combinatorial logic blocks 26 and 27.

2. Load the outputs of the combinatorial logic to the shift register latches in banks 24 and 25 by enabling the master and slave clocks.

3. Clock the output data produced by the combinatorial logic out via the scan output 206 by enabling the scan and slave clocks. Compare the data with that expected from the test pattern originally input to evaluate functionality of the device.

[0018] It will be realized that although this procedure has simplified testing in that no overall sequence of test patterns sufficient to test the device fully needs to be designed or generated, there is still the need to specify test patterns adequate to exercise the combinatorial blocks which remains a significant task and, in testing an individual production device, there is the need to generate these test patterns and apply them to a device under test.

[0019] Consider now that a production device is to be

subject to an accelerated life test. A device under test is placed in an environmental chamber capable of providing the high stress environment for the test to proceed. What is required now is that the individual device be subjected to the specified environment whilst it is being functionally exercised. To provide the excitation in accordance with the prior art, signal generation means is provided within the chamber and arranged to provide a pre-determined sequence of signals to exercise the device.

[0020] By contrast, in accordance with the present invention two of the outputs 31 of a scannable chain of shift register latches 32 (Figure 3) are connected to an exclusive-OR gate 35. A multiplexer 36 under the control of an exercise register 37 is provided so that the output of the exclusive-OR gate may be fed back directly to the scan input of the shift register latch chain 32. The effect of this connection is to provide a linear feedback shift register arrangement. As is known in the art (see for example Horowitz and Hill, "The Art of Electronics", Cambridge University Press, 1980 (p.438-9)) a linear feedback shift register is capable of providing a pseudo random binary sequence. Hence it will be realized that, with the circuit configured as aforesaid, the shift register constituted by the scan path of shift register latches itself behaves as a pattern generator applying a plurality of changing inputs 31 to subsequent combinatorial logic. Exercise of the device can be achieved by feeding no more than simple input (power supply and scan and slave clock signals) to the device whilst undergoing an accelerated life test. By monitoring the overall scan output (for example, 206 of the device of Figure 2) then a dynamic signal providing confirmation of operation may be monitored. The exercise of the device may be controlled via a control input 37 in a way analogous to entering the test mode.

[0021] A circuit implementation of an exclusive-OR gate is illustrated in Figure 4, wherein shift register latch feedback signals 405 and 406 are connected to NAND gates 401 and 402 and inverters 403 and 404. The outputs of NAND gates 401 and 402 are further connected to a NAND gate 400 so as to realize the exclusive-OR function. A multiplexer is provided by a gate network 47 in conjunction with inverter 46 so that either the output of NAND gate 400 or the normal scan input connected to input 48 (*cf.* 33 of Figure 3) may be fed to a shift register latch 40 dependent upon the state of control input 49. Shift register latch 40 is the first latch in the scan path of the device.

[0022] Since a linear feedback shift register will fail to generate a pseudo random binary sequence in the event that it has all zeros as an initial value, in designs where this is possible, it must be accommodated. To this end in the present embodiment the first shift register latch 40 (not constituting part of the functional arrangement of the circuit) is forced with an initial high value 41 when the circuit is re-set by using the re-set signal as the master clock on input 42. It will be appreciated that in some embodiments this stage will not be required. When scanning is to occur, the scan clock and slave clocks may be applied in the way described to inputs 43 and 44 to generate the first scan output in the chain (45).

[0023] It will be appreciated that the same technique may be applied to devices with multiple scan paths in the same device either by providing that the scan paths are configurable in series, or by arranging the shift register latch chain as a plurality of linear feedback shift registers.

[0024] The ability to self exercise has been provided to an integrated logic circuit with a very small overhead in device layout. In many embodiments only an exclusive-OR gate and a multiplexer are required to add this feature to the device, which is a very small device area.

[0025] The technique described above may be applied to any scan chain, including those formed between devices. In this case the exclusive-OR and multiplex functions may be provided as part of one of the interconnected devices or externally. An assembled circuit board having boundary scannable device may thus be subjected to a self exercised accelerated life test.

[0026] An alternative embodiment of an integrated logic device will now be considered.

[0027] A block diagram of a logic device integrated onto a single substrate in shown in Figure 5. The device is a frame processing accelerator for use in conjunction with a local area network adaptor. The precise functionality of the device does not form part of the present invention, however it will be observed that the device includes a microcontroller 50 (implementing datapath manipulation, control of static random access memory and scheduling), a local bus interface 51 (performing bus arbitration, control and parity checking), monitoring logic 52 (in particular packet header receive and transmit monitoring and system direct memory access monitoring), a phase locked loop clock generator 53 for deriving internal clocks from external inputs and some control registers 54. A plurality of inputs and outputs 55 are designated as shown. Some portions of the device relevant to understanding of the present invention will now be described in more detail.

[0028] Gating logic 60 (Figure 6) generates internal main clock FLP, slave clock FHP and scan clock FSP signals from a main clock input MBCLK1. The clock generators may be held at a particular level by applying a suitable signal to the reset input MRESET. Clock generation is controlled with respect to two control inputs MANT0, MANT1 which gate either the master clock FLP or the scan clock FSP to the shift register latches (not shown but hereinbefore described). It will be noted in particular that when MANT1 is high and MANT0 is low, the scan (FSP) and slave (FHP) clocks are operative. In other words, the device is in the scan test mode.

[0029] In accordance with design for test practice, the clock signals FLP, FHP and FSP are fed to device shift register latches, for example, shift register latch 71 (Figure 7). Further shift register latches 72, 73, 74 are shown

connected in a scan chain as hereinbefore described. Scan outputs from shift register latches 72 and 73 are fed back to the scan input of a first shift register latch 70 via Exclusive-OR gating 78 and selector gates 79. In this way, the shift register latches behave as a linear feedback shift register and self excitation of the device is possible provided appropriate signal levels are applied to selector gates (input MADL01) to disable normal input MBGR and enable the feedback. Shift register latch 70 receives a high input I_1 and the reset signal as master clock so that the linear feedback shift register is always loaded with a non zero initial value as previously described.

[0030] The scan output 75 of the last shift register latch 74 is fed to an output SBRLSN via a selector gate 76. The selector is controlled by the output of gates of logic 77. It will be noted that when MANT1 is high and MANT0 is low (the test condition) then the normal pin output SBRLS is disabled and the scan output appears at SBRLSN.

[0031] Figure 8 represents external components to which the device needs to be connected to exercise itself. Typically, these components may be mounted on an environmental test chamber fixture, for example, a printed circuit board to be placed in the chamber. The components are principally resistors, for example, resistor 81 connected to pull up the inputs of the device to one of two power supplies (PS1, PS2). Alternatively, some pins are directly connected to ground. A capacitor is connected between pin PLLCAP and ground to provide a feedback capacitor for the on board phase locked loop clock generator 53. Further, a clock signal generator 83 provides an input to the clock input pin MBCLK1.

[0032] It will be appreciated that this small number of external components is all that is required to provide an exercised device to which an accelerated life test may be given. This will be contrasted with the prior art, where test pattern generators would be required either on the fixture or connected from outside the environmental chamber.

[0033] To effect a burn-in test, the fixture is placed in a test chamber, the test conditions established and the device energised.

[0034] The invention is also applicable to integrated logic circuits including an integrated device interconnected with other circuit components.

Claims

1. An integrated logic circuit, wherein a plurality of storage elements are configurable as at least part of a scan path including a feedback from elements in the path to a previous element operable to provide a pseudo random binary sequence for exercising the integrated logic circuit during testing, characterized in that:

   each of the plurality of storage elements (21-25) has an input for a master clock signal (MASTER), an input for a slave clock signal (SLAVE) and an input for a scan clock signal (SCAN), an input for normal data (I1) responsive to the master clock signal and an input for scan data (Is) responsive to the scan clock signal,

   wherein each of the plurality of storage elements (21-25) operates in a normal mode when the master clock signal and the slave clock signal are active, and each of the plurality of storage elements (21-25) operates in a scan mode when the scan clock signal and the slave clock signal are active.

2. A method for exercisinq a plurality of integrated logic circuits during an accelerated life test wherein each of the plurality of integrated logic circuits have a plurality of storage elements which are configurable as at least part of a scan path including a feedback from elements in the path to a previous element operable to provide a pseudo random binary sequence for exercising the integrated logic circuit during testing, characterized by:

   modifying a plurality of storage elements (21-25) , each of said storage elements being as defined in claim 1, which form at least a portion of functional logic used during normal operation of the integrated circuit to form an interconnected shift register by adding a scan clock input (SCAN) and an input for scan data (Is) to each of the plurality of storage elements,

   operating the plurality of integrated circuits in a high stress environment by providing only fixed voltage levels (PS1, PS2) and clock signal (83) to the plurality of integrated circuits, and

   monitoring an output of the shift register (MONITOR) of each of the plurality of integrated circuits to verify correct operation responsive to the pseudo random binary sequence of each of the plurality of integrated circuits during operation in the high stress environment.

3. The method of claim 2, further characterized in that a majority of functional logic circuits of each of the plurality of integrated circuits are exercised in response to the pseudo random binary sequence.

Patentansprüche

1. Integrierte Logikschaltung, bei der mehrere Speicherelemente wenigstens als Teil eines Scan-Pfades konfigurierbar sind, der eine Rückführung von Elementen in dem Pfad zu einem vorhergehenden Element aufweist, das so betrieben werden kann,

daß es eine pseudostatistische binäre Sequenz zum Prüfen der integrierten Logikschaltung während des Testens liefert, dadurch gekennzeichnet, daß:

jedes der mehreren Speicherelemente (21-25) einen Eingang für ein Haupttaktsignal (MASTER), einen Eingang für ein untergeordnetes Taktsignal (SLAVE) und einen Eingang für ein Scan-Taktsignal (SCAN), einen Eingang für normale Daten (I1), der auf das Haupttaktsignal reagiert, und einen Eingang für Scan-Daten (Is) umfaßt, der auf das Scan-Taktsignal reagiert, wobei jedes der mehreren Speicherelemente (21-25) in einem normalen Modus arbeitet, wenn das Haupttaktsignal und das untergeordnete Taktsignal aktiv sind und jedes der mehreren Speicherelemente (21-25) in einem Scan-Modus arbeitet, wenn das Scan-Taktsignal und das untergeordnete Taktsignal aktiv sind.

2. Verfahren zum Prüfen mehrerer integrierter Logikschaltungen während eines beschleunigten Lebensdauertests, bei dem jede der mehreren integrierten Logikschaltungen mehrere Speicherelemente aufweist, die wenigstens als Teil eines Scan-Pfades konfigurierbar sind, der eine Rückführung von Elementen in dem Pfad zu einem vorhergehenden Element umfaßt, das so betrieben werden kann, daß es eine pseudostatistische binäre Sequenz zum Prüfen der integrierten Logikschaltung während des Testens liefert, dadurch gekennzeichnet, daß:

die mehreren wie im Anspruch 1 definierten Speicherelemente (21-25), die wenigstens einen Teil der während des normalen Betriebs der integrierten Schaltung verwendeten Funktionslogik bilden, durch Hinzufügen eines Scan-Takteingangs (SCAN) und eines Eingangs (Is) für Scan-Daten zu jedem der mehreren Speicherelemente so modifiziert werden, daß sie ein verbundenes Schieberegister bilden,
die mehreren integrierten Schaltungen in einer Umgebung hoher Beanspruchung betrieben werden, indem nur festgelegte Spannungspegel (PS1, PS2) und ein Taktsignal (83) an die mehreren integrierten Schaltungen angelegt werden, und
ein Ausgang (MONITOR) des Schieberegisters jeder der mehreren integrierten Schaltungen überwacht wird, um die korrekte Arbeitsweise als Reaktion auf die pseudostatistische binäre Sequenz jeder der mehreren integrierten Schaltungen während des Betriebs in einer Umgebung hoher Beanspruchung nachzuprüfen.

3. Verfahren nach Anspruch 2, darüber hinaus dadurch gekennzeichnet, daß die Mehrzahl der Funktionslogikschaltungen jeder der mehreren integrierten Schaltungen als Reaktion auf die pseudostatistische binäre Sequenz geprüft wird.

Revendications

1. Circuit logique intégré dans lequel une pluralité d'élements de stockage sont configurables sous la forme d'au moins une partie de trajet d'analyse incluant une rétroaction à partir d'éléments dans le trajet vers un élément précédent pouvant fonctionner pour obtenir une séquence binaire pseudo aléatoire pour mettre en oeuvre le circuit logique intégré au cours d'un contrôle, caractérisé en ce que:

chacun de la pluralité d'éléments de stockage (21 - 25) a une entrée pour un signal d'horloge maître (MASTER), une entrée pour un signal d'horloge esclave (SLAVE) et une entrée pour un signal d'horloge d'analyse (SCAN), une entrée pour des données normales (II) sensibles au signal d'horloge maître et une entrée pour des données d'analyse (Is) sensibles au signal d'horloge d'analyse,
dans lequel chacun de la pluralité d'éléments de stockage (21 - 25) fonctionne dans un mode normal lorsque le signal d'horloge maître et le signal d'horloge esclave sont actifs, et chacun de la pluralité d'éléments de stockage (21 - 25) fonctionne dans un mode d'analyse lorsque le signal d'horloge d'analyse et le signal d'horloge esclave sont actifs.

2. Procédé pour mettre en oeuvre une pluralité de circuits logiques intégrés au cours d'un contrôle d'endurance accéléré, dans lequel chacun de la pluralité de circuits logiques intégrés comporte une pluralité d'éléments de stockage qui sont configurables sous la forme d'au moins une partie d'un trajet de balayage, y compris une rétroaction à partir d'éléments dans le trajet vers un élément précédent pouvant fonctionner pour obtenir une séquence binaire pseudo aléatoire pour mettre en oeuvre le circuit logique intégré au cours d'un contrôle, caractérisé par :

la modification d'une pluralité d'éléments de stockage (21 - 25), chacun desdits éléments de stockage étant tel que défini dans la revendication 1, qui forment au moins une partie d'une logique fonctionnelle utilisée au cours d'un fonctionnement normal du circuit intégré pour former un registre à décalage interconnecté,

par addition d'une entrée d'horloge d'analyse (SCAN) et d'une entrée pour des données d'analyse (Is), à chacun de la pluralité d'éléments de stockage,

l'actionnement de la pluralité de circuits intégrés dans un environnement de contrainte élevée en fournissant uniquement des niveaux de tension fixes (PS1, PS2) et un signal d'horloge (83) à la pluralité de circuits intégrés, et

la surveillance d'une sortie du registre à décalage (MONITOR) de chacun de la pluralité de circuits intégrés pour vérifier un fonctionnement correct sensible à la séquence binaire pseudo aléatoire de chacun de la pluralité de circuits intégrés au cours du fonctionnement dans l'environnement de contrainte élevée

3. Procédé selon la revendication 2, caractérisé en outre en ce qu'une majorité de circuits logiques fonctionnels de chacun de la pluralité de circuits intégrés sont mis en oeuvre en réponse à la séquence binaire pseudo aléatoire.

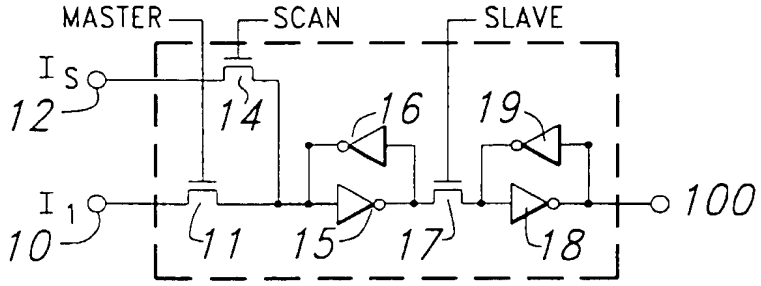
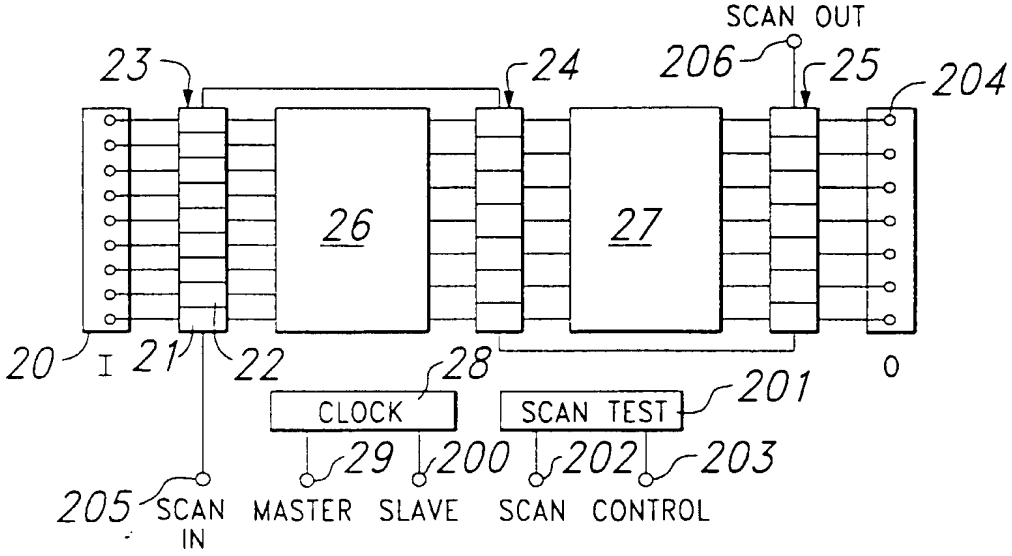

MASTER
SCAN
SLAVE
I S
12
14
16
19
I 1
10
11
15
17
18
100

Fig. 1


SCAN OUT
23
24
206
25
204
26
27
20
I
21
22
28
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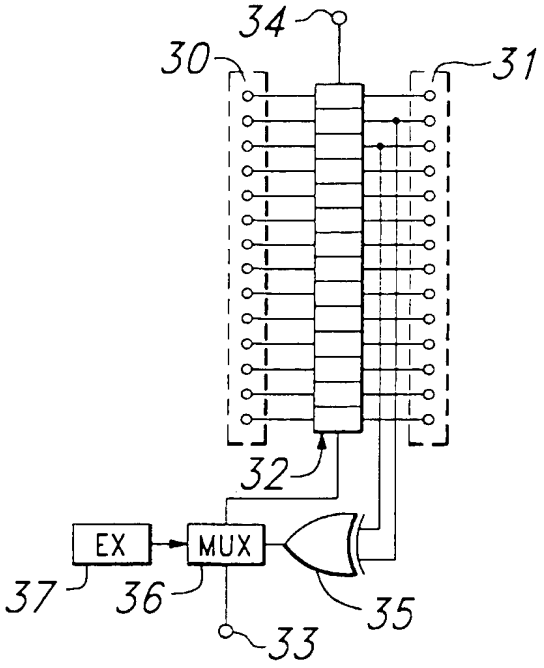
CLOCK
SCAN TEST
201
29
200
202
203
205
SCAN IN
MASTER
SLAVE
SCAN CONTROL

Fig. 2


34
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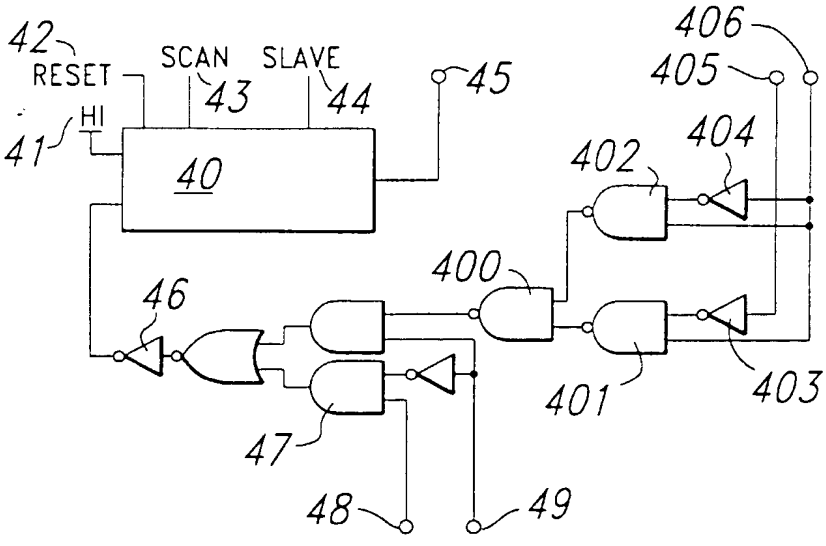
31
32
EX
MUX
37
36
35
33

Fig. 3


42
RESET
SCAN
SLAVE
43
44
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HI
41
40
406
405
404
402
400
46
401
403
47
48
49

Fig. 4

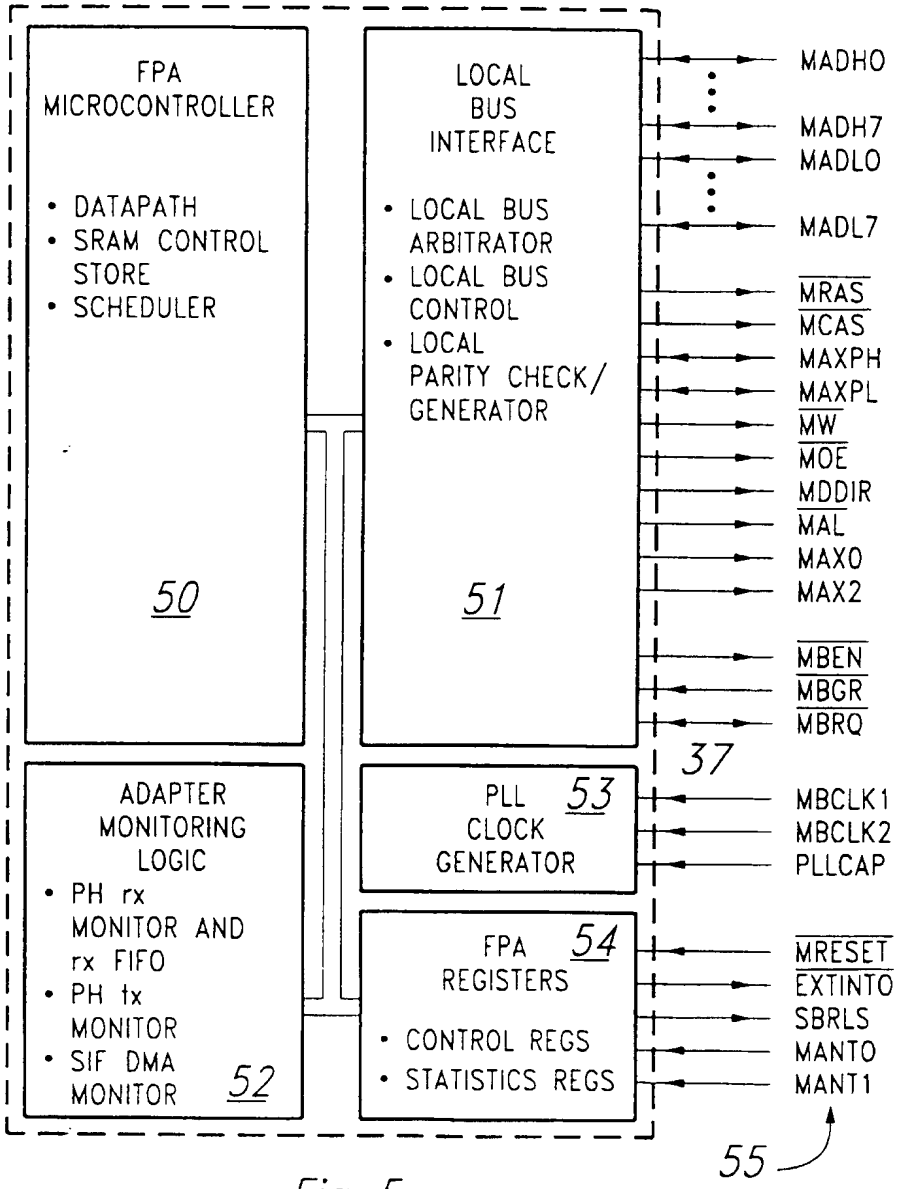
FPA
MICROCONTROLLER
• DATAPATH
• SRAM CONTROL STORE
• SCHEDULER
50
LOCAL
BUS
INTERFACE
• LOCAL BUS ARBITRATOR
• LOCAL BUS CONTROL
• LOCAL PARITY CHECK/ GENERATOR
51
ADAPTER
MONITORING
LOGIC
• PH rx MONITOR AND rx FIFO
• PH tx MONITOR
• SIF DMA MONITOR
52
PLL 53
CLOCK
GENERATOR
FPA 54
REGISTERS
• CONTROL REGS
• STATISTICS REGS
MADH0
MADH7
MADL0
MADL7
MRAS
MCAS
MAXPH
MAXPL
MW
MOE
MDDIR
MAL
MAX0
MAX2
MBEN
MBGR
MBRQ
37
MBCLK1
MBCLK2
PLLCAP
MRESET
EXTINTO
SBRLS
MANTO
MANT1
55

Fig. 5

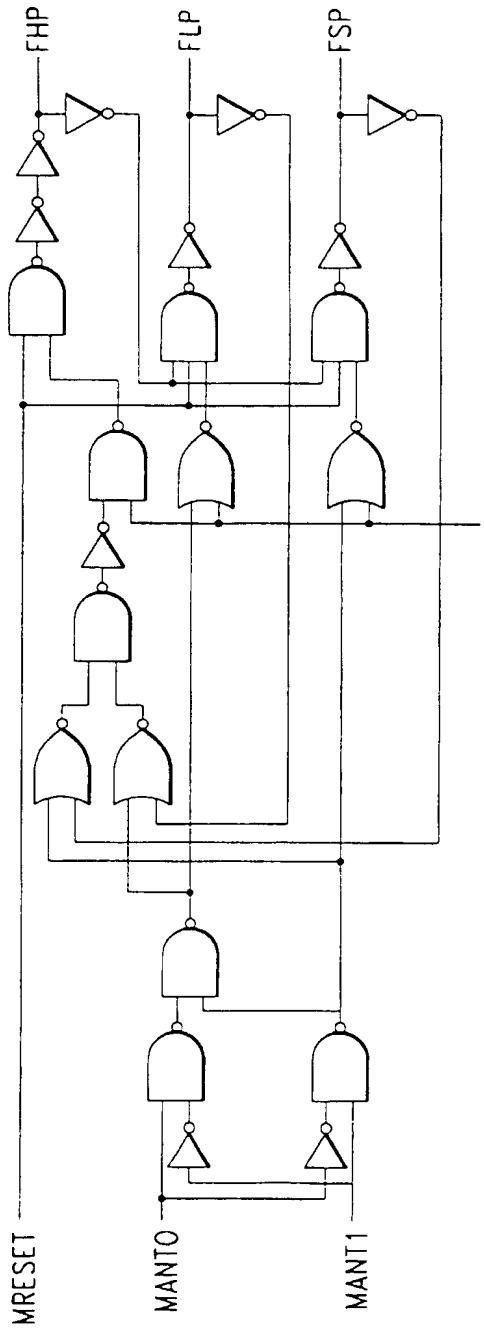

Fig. 6

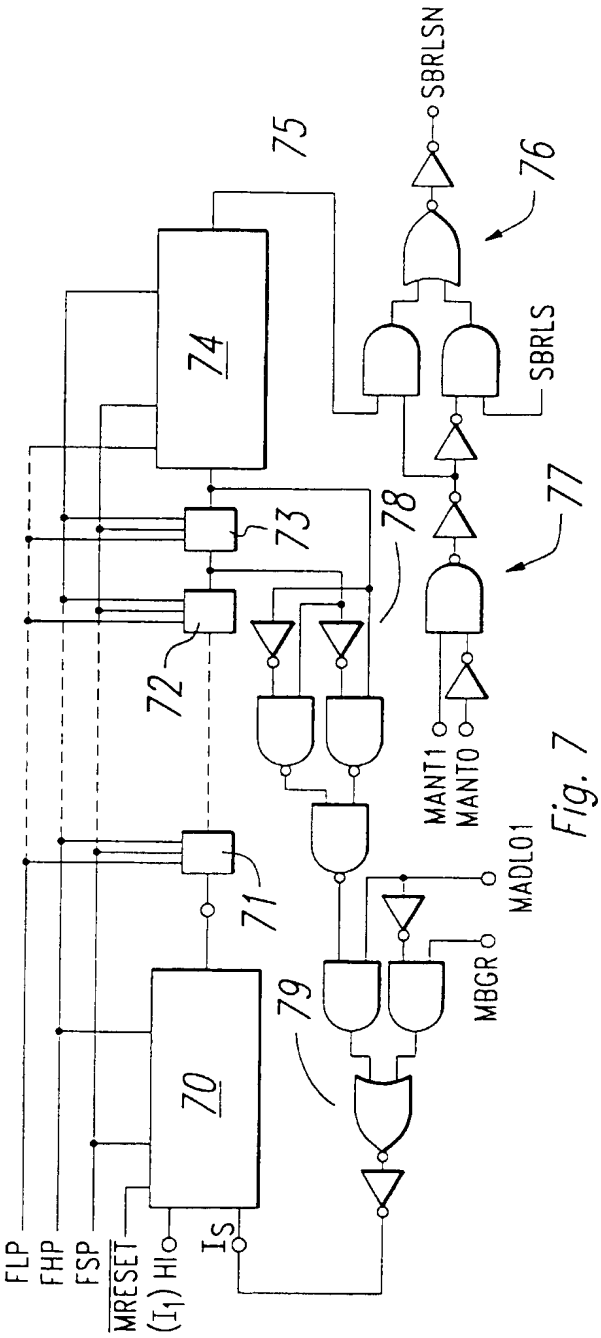
SBRLSN
75
76
74
SBRLS
77
73
78
72
MANT1
MANT0
71
MADL01
MBGR
79
70
FLP
FHP
FSP
MRESET
(I1) HI
IS

Fig. 7

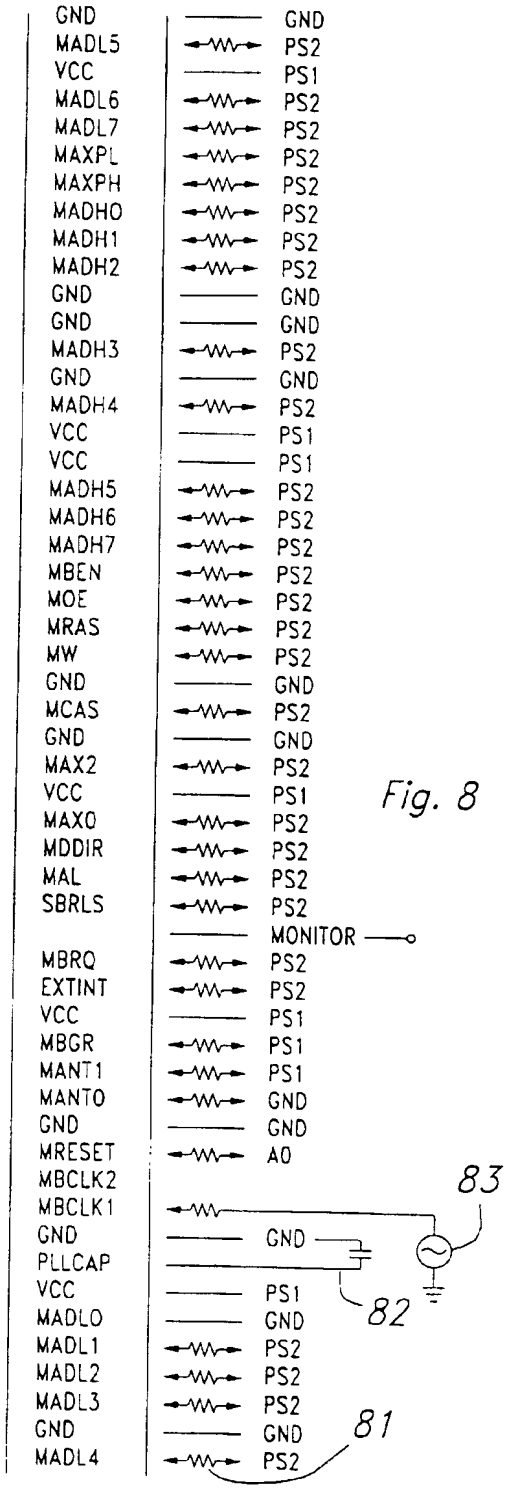
GND
MADL5
VCC
MADL6
MADL7
MAXPL
MAXPH
MADHO
MADH1
MADH2
GND
GND
MADH3
GND
MADH4
VCC
VCC
MADH5
MADH6
MADH7
MBEN
MOE
MRAS
MW
GND
MCAS
GND
MAX2
VCC
MAXO
MDDIR
MAL
SBRLS
MBRQ
EXTINT
VCC
MBGR
MANT1
MANTO
GND
MRESET
MBCLK2
MBCLK1
GND
PLLCAP
VCC
MADLO
MADL1
MADL2
MADL3
GND
MADL4
GND
PS2
PS1
MONITOR
A0
83
82
81

Fig. 8